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File 8:EI Compendex(R) 1884-2010/Mar W2  
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File 99:Wilson Appl. Sci & Tech Abs 1983-2010/Jan  
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Set	Items	Description
S1	587060	(ADDRESS? ? OR (WEB OR FTP OR WWW OR HTTP) (1W) SERVER? ? OR NAME? ? (1N) SERVER? ? OR DNS OR (IP OR INTERNET() PROTOCOL) () ADDRESS? ? OR (HOST OR DOMAIN) () NAME? ? OR SERVER() (ID OR IDENTIFICATION))
S2	41769	S1(3N) (DETERMIN??? OR DEFIN??? OR SET OR ESTABLISH??? OR SELECT??? OR LIMIT? ? OR LIMITATION? ? OR DECID??? OR CHECK? OR TEST? OR EXAMIN? OR ANALYZ? OR ANALYS? OR ASSESS? OR IDENTIF? OR SCRUTINIZ? OR SCRUTINIS? OR EVALUAT???)
S3	32733	(POSITION? ? OR LOCATION? ? OR OFFSET OR OFF() SET) (3N) (FIELD? ? OR DATA(3W) (STRUCTURE? ? SCHEMA? ? OR MODEL? ?))
S4	7	S2(5N) S3
S5	3287	(INDEX?? OR INDICE? ?) (3N) ARRAY? ?
S6	2	S2(5N) S5
S7	38	S2 AND S3
S8	25	RD (unique items)
S9	9	S8 AND PY=1963:2003
S10	9	S2 AND S5
S11	7	RD (unique items)

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## Subject summary

? t/ 5,k/ all

### Dialog eLink:

USPTO Full Text Retrieval Options

11/5,K/1 (Item 1 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

(c) 2010 Elsevier Eng. Info. Inc. All rights reserved.

0018483571 E.I. COMPENDEX No: 20083211448379

Index-BitTableFI: An improved algorithm for mining frequent itemsets

Song, Wei; Yang, Bingru; Xu, Zhangyan

**Corresp. Author/ Affil:** Song, W.: College of Information Engineering, North China University of Technology, Beijing, 100144, China

**Corresp. Author email:** sgyzfr@yahoo.com.cn

Knowledge-Based Systems ( Knowl Based Syst ) ( Netherlands ) 2008 21/6 (507-513)

**Publication Date:** 20080101

**Publisher:** Elsevier

**CODEN:** KNSYE **ISSN:** 0950-7051

**Publisher Item Identifier:** S0950705108000531

**Item Identifier (DOI):** [10.1016/j.knsys.2008.03.011](https://doi.org/10.1016/j.knsys.2008.03.011)

**Document Type:** Article; Journal **Record Type:** Abstract

**Language:** English **Summary Language:** English

**Number of References:** 25

Efficient algorithms for mining frequent itemsets are crucial for mining association rules as well as for many other data mining tasks. Methods for mining frequent itemsets have been implemented using a BitTable structure. BitTableFI is such a recently proposed efficient BitTable-based algorithm, which exploits BitTable both horizontally and vertically. Although making use of efficient bit wise operations, BitTableFI still may suffer from the high cost of candidate generation and **test**. To **address** this problem, a new algorithm Index-BitTableFI is proposed. Index-BitTableFI also uses BitTable horizontally and vertically. To make use of BitTable horizontally, **index array** and the corresponding computing method are proposed. By computing the subsume index, those itemsets that co-occurrence with representative item can be identified quickly by using breadth-first search at one time. Then, for the resulting itemsets generated through the **index array**, depth-first search strategy is used to generate all other frequent itemsets. Thus, the hybrid search is implemented, and the search space is reduced greatly. The advantages of the proposed methods are as follows. On the one hand, the redundant operations on intersection of tidsets and frequency-checking can be avoided greatly; On the other hand, it is proved that frequent itemsets, including representative item and having the same supports as representative item, can be identified directly by connecting the representative item with all the combinations of items in its subsume index. Thus, the cost for processing this kind of itemsets is lowered, and the efficiency is improved. Experimental results show that the proposed algorithm is efficient especially for dense datasets. (c) 2008 Elsevier B.V. All rights reserved.

**Descriptors:** Algorithms; Associative processing; Boolean functions; Data mining; Decision support systems; Information management; Knowledge management; Search engines; \* Mining

**Identifiers:** Bit wise operations; Breadth-first search (BFS); Candidate generation; Co-occurrence; Computing methods; Data mining tasks; Data-sets; Depth-first search (DFS); Efficient algorithms; Frequent Itemsets; Hybrid search; Improved algorithm; Itemsets; Mining association rules; Mining frequent itemsets; New algorithm; Search spaces

**Classification Codes:**

502.1 (Mine & Quarry Operations)

721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory))

723.2 (Data Processing)

723.5 (Computer Applications)

912.2 (Management)

723 (Computer Software, Data Handling & Applications)

...bit wise operations, BitTableFI still may suffer from the high cost of candidate generation and **test**. To **address** this problem, a new algorithm Index-BitTableFI is proposed. Index-BitTableFI also uses BitTable horizontally and vertically. To make use of BitTable horizontally, **index array** and the corresponding computing method are proposed. By computing the subsume index, those itemsets that... using breadth-first search at one time. Then, for the resulting itemsets generated through the **index array**, depth-first search strategy is used to generate all other frequent itemsets. Thus, the hybrid ...

**Descriptors:**

**Dialog eLink:**

**USPTO Full Text Retrieval Options**

11/5,K/2 (Item 2 from file: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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0018372197 **E.I. COMPENDEX No:** 20082211289304  
**Index-maxminer: A new maximal frequent itemset mining algorithm**

Song, Wei; Yang, Bingru; Xu, Zhangyan  
**Corresp. Author/ Affil:** Song, W.: College of Information Engineering, North China University of Technology,  
Beijing, 100144, China

**Corresp. Author email:** sgzyfr@yahoo.com.cn

**Author email:** bryang kd@yahoo.com.cn; xyzwlx72@yahoo.com.cn

International Journal on Artificial Intelligence Tools ( Int. J. on Artif. Intell. Tools ) ( Singapore ) 2008 17/2  
(303-320)

**Publication Date:** 20080609

**Publisher:** World Scientific Publishing Co. Pte. Ltd

**ISSN:** 0218-2130

**Publisher Item Identifier:** S021821300800390X

**Item Identifier (DOI):** 10.1142/S021821300800390X

**Document Type:** Article; Journal **Record Type:** Abstract

**Treatment:** T; (Theoretical)

**Language:** English **Summary Language:** English

**Number of References:** 28

Because of the inherent computational complexity, mining the complete frequent item-set in dense datasets remains to be a challenging task. Mining Maximal Frequent Item-set (MFI) is an alternative to **address** the problem. Set-Enumeration Tree (SET) is a common data structure used in several MFI mining algorithms. For this kind of algorithm, the process of mining MFIs can also be viewed as the process of searching in set-enumeration tree. To reduce the search space, in this paper, a new algorithm, Index-MaxMiner, for mining MFI is proposed by employing a hybrid search strategy blending breadth-first and depth-first. Firstly, the **index array** is proposed, and based on bitmap, an algorithm for computing **index array** is presented. By adding subsume index to frequent items, Index-MaxMiner discovers the candidate MFIs using breadth-first search at one time, which avoids first-level nodes that would not participate in the answer set and reduces drastically the number of candidate itemsets. Then, for candidate MFIs, depth-first search strategy is used to generate all MFIs. Thus, the jumping search in SET is implemented, and the search space is reduced greatly. The experimental results show that the proposed algorithm is efficient especially for dense datasets. (c) 2008 World Scientific Publishing Company.

**Descriptors:** Algorithms; Association rules; Trees (mathematics); \*Data mining

**Identifiers:** **Index array**; Maximal frequent itemset; Set-enumeration tree

**Classification Codes:**

723.2 (Data Processing)

903.1 (Information Sources & Analysis)

921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory)

...to be a challenging task. Mining Maximal Frequent Item-set (MFI) is an alternative to **address** the problem.

Set-Enumeration Tree (SET) is a common data structure used in several MFI mining algorithms. For ...

...proposed by employing a hybrid search strategy blending breadth-first and depth-first. Firstly, the **index array** is proposed, and based on bitmap, an algorithm for computing **index array** is presented. By adding subsume index to frequent items, Index-MaxMiner discovers the candidate MFIs...

**Descriptors:**

**Identifiers:** **Index array**; Maximal frequent itemset; Set-enumeration tree

**Dialog eLink:**

**USPTO Full Text Retrieval Options**

11/5,K/3 (Item 3 from file: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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0014636919 **E.I. COMPENDEX No:** 2000405291727  
**1.6 ns access, 1 GHz two-way set-predicted and sum-indexed 64-kByte data cache**

Silberman, Joel; Aoki, Naoaki; Kojima, Nobuo; Dhong, Sang

**Corresp. Author/ Affil:** Silberman, Joel: IBM T.J. Watson Research Cent, Yorktown Heights, United States

**Conference Title:** 2000 Symposium on VLSI Circuits

**Conference Location:** Honolulu, HI, USA **Conference Date:** 20000615-20000617

**E.I. Conference No.:** 57181

IEEE Symposium on VLSI Circuits, Digest of Technical Papers ( IEEE Symp VLSI Circuits Dig Tech Pap ) 2000  
(220-221)

**Publication Date:** 20001203

**Publisher:** IEEE

**CODEN:** 85PXA

**Document Type:** Conference Paper; Conference Proceeding **Record Type:** Abstract

**Treatment:** T; (Theoretical)

**Language:** English **Summary Language:** English

**Number of References:** 4

Designed to support two cycle execution of load instructions in a 1 GHz single issue, in order, 64-bit reduced instruction set computing (RISC) processor, a 64-kByte, two-way set associative 1.6 ns access, 1 GHz pipelined data cache features up to 16-byte input/output (I/O) to the processor, 128-byte single cycle transfer for reload and cast out operations, and internal forwarding of data for loads that closely follow stores. Cache access is supported by a 512-entry, two-way **set** associative **address** translation array and a two read-, one write-port directory that can support bus snoop requests on the second read port.

**Descriptors:** Associative processing; Associative storage; Buffer storage; Decoding; Input output programs; Reduced instruction set computing; \*VLSI circuits

**Identifiers:** **Set** associative **address** translation array; Sum **indexed** data cache

**Classification Codes:**

714.2 (Semiconductor Devices & Integrated Circuits)

722.1 (Data Storage, Equipment & Techniques)

723.1 (Computer Programming)

723.2 (Data Processing)

...loads that closely follow stores. Cache access is supported by a 512-entry, two-way **set** associative **address** translation array and a two read-, one write-port directory that can support bus snoop...

**Descriptors:**

**Identifiers:** **Set** associative **address** translation array; Sum **indexed** data cache

**Dialog eLink:**

**USPTO Full Text Retrieval Options**

11/5,K/4 (Item 1 from file: 2)

DIALOG(R)File 2: INSPEC

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11130614

**Title:** Index-BitTableFI: an improved algorithm for mining frequent itemsets

**Author(s):** Wei Song; Bingru Yang; Zhangyan Xu

**Author Affiliation:** Coll. of Inf. Eng., North China Univ. of Technol., Beijing, China

**Journal:** Knowledge-Based Systems, vol.21, no.6, pp.507-13

**Publisher:** Elsevier Science Ltd.

**Country of Publication:** UK

**Publication Date:** Aug. 2008

**ISSN:** 0950-7051

**CODEN:** KNSYET

**Document Number:** S0950-7051(08)00053-1

**Item Identifier (DOI):** [10.1016/j.knosys.2008.03.011](https://doi.org/10.1016/j.knosys.2008.03.011)

**Language:** English

**Document Type:** Journal Paper (JP)

**Treatment:** Practical (P); Theoretical or Mathematical (T)

**Abstract:** Efficient algorithms for mining frequent itemsets are crucial for mining association rules as well as for many other data mining tasks. Methods for mining frequent itemsets have been implemented using a BitTable structure. BitTableFI is such a recently proposed efficient BitTable-based algorithm, which exploits BitTable both horizontally and vertically. Although making use of efficient bit wise operations, BitTableFI still may suffer from the high cost of candidate generation and **test**. To **address** this problem, a new algorithm Index-BitTableFI is proposed. Index-BitTableFI also uses BitTable horizontally and vertically. To make use of BitTable horizontally, **index array** and the corresponding computing method are proposed. By computing the subsume index, those itemsets that co-occurrence with representative item can be identified quickly by using breadth-first search at one time. Then, for the resulting itemsets generated through the **index array**, depth-first search strategy is used to generate all other frequent itemsets. Thus, the hybrid search is implemented, and the search space is reduced greatly. The advantages of the proposed methods are as follows. On the one hand, the redundant operations on intersection of tidsets and frequency-checking can be avoided greatly; On the other hand, it is proved that frequent itemsets, including representative item and having the same supports as representative item, can be identified directly by connecting the representative item with all the combinations of items in its subsume index. Thus, the cost for processing this kind of itemsets is lowered, and the efficiency is improved. Experimental results show that the proposed algorithm is efficient especially for dense datasets. [All rights reserved Elsevier]. (25 refs.)

**Subfile(s):** C (Computing & Control Engineering)

**Descriptors:** data mining; data structures; database indexing; tree searching

**Identifiers:** Index-BitTableFI frequent itemset mining algorithm; association rule mining; data mining; BitTable

structure; bit wise operation; **index array** structure; breadth-first search strategy

**Classification Codes:** C6170K (Knowledge engineering techniques); C1160 (Combinatorial mathematics); C6120 (File organisation); C6160 (Database management systems (DBMS))

**INSPEC Update Issue:** 2008-034

**Copyright:** 2008, The Institution of Engineering and Technology

**Abstract:** ...bit wise operations, BitTableFI still may suffer from the high cost of candidate generation and **test**. To **address** this problem, a new algorithm Index-BitTableFI is proposed. Index-BitTableFI also uses BitTable horizontally and vertically. To make use of BitTable horizontally, **index array** and the corresponding computing method are proposed. By computing the subsume index, those itemsets that... using breadth-first search at one time. Then, for the resulting itemsets generated through the **index array**, depth-first search strategy is used to generate all other frequent itemsets. Thus, the hybrid ...

**Identifiers:** ...BitTableFI frequent itemset mining algorithm; association rule mining; data mining; BitTable structure; bit wise operation; **index array** structure; breadth-first search strategy

**Dialog eLink:**

**USPTO Full Text Retrieval Options**

11/5,K/5 (Item 2 from file: 2)

DIALOG(R)File 2: INSPEC

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05580578

**Title:** A quantitative evaluation of cache types for high-performance computer systems

**Author(s):** Wu, C.E.; Hsu, Y.; Liu, Y.-H.

**Author Affiliation:** IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA

**Journal:** IEEE Transactions on Computers , vol.42 , no.10 , pp.1154-62

**Country of Publication:** USA

**Publication Date:** Oct. 1993

**ISSN:** 0018-9340

**CODEN:** ITCOB4

**U.S. Copyright Clearance Center Code:** 0018-9340/93/\$03.00

**Item Identifier (DOI):** [10.1109/12.257701](https://doi.org/10.1109/12.257701)

**Language:** English

**Document Type:** Journal Paper (JP)

**Treatment:** Practical (P)

**Abstract:** Parallel accesses to the table lookaside buffer (TLB) and cache array are crucial for high-performance computer systems, and the choice of cache types is one of the most important factors affecting cache performance. The authors classify caches according to both index and tag. Since both index and tag could be either virtual (V) or real (R), their classification results in four combinations or cache types. The real address caches with virtual tags for high-performance computer systems in this study are prediction-based, since index bins are generated from a small array and predictions could be false. As a result, they also discuss and **evaluate** real address MRU caches with real tags, and propose virtually indexed MRU caches with real tags. Each of the four cache types and MRU caches are discussed and evaluated using trace-driven simulation. The results show that a virtually indexed MRU cache with real tags is a good choice for high-performance computer systems ( 27 refs.)

**Subfile(s):** C (Computing & Control Engineering)

**Descriptors:** buffer storage; performance evaluation

**Identifiers:** cache types; table lookaside buffer; high-performance computer; cache **array**; **index**; tag; virtual; real; prediction-based

**Classification Codes:** C5310 (Storage system design); C5470 (Performance evaluation and testing)

**INSPEC Update Issue:** 1994-002

**Copyright:** 1994, IEE

**Abstract:** ...a small array and predictions could be false. As a result, they also discuss and **evaluate** real address MRU caches with real tags, and propose virtually indexed MRU caches with real tags. Each...

**Identifiers:** cache types; table lookaside buffer; high-performance computer; cache **array**; **index**; tag; virtual; real; prediction-based

**Dialog eLink:**

**USPTO Full Text Retrieval Options**

11/5,K/6 (Item 3 from file: 2)

DIALOG(R)File 2: INSPEC

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01759374

**Title:** Automatic partial deletion of high-speed buffer entries

**Author(s):** Ahearn, T.P.; Gannon, P.M.; Liptay, J.S.; Unterberger, R.M.

**Author Affiliation:** IBM, New York, NY, USA

**Journal:** IBM Technical Disclosure Bulletin , vol.17 , no.7 , pp.2038-9

**Country of Publication:** USA

**Publication Date:** Dec. 1974

**ISSN:** 0018-8689

**CODEN:** IBMTAA

**Language:** English

**Document Type:** Journal Paper (JP)

**Treatment:** Practical (P)

**Abstract:** A mechanism is described which automatically deletes portions of a highspeed buffer on the occurrence of a buffer data error or an address compare error. Although only two types of errors are described, the choice was arbitrary and other types of errors may be included in the disabling process. The logic shown permits a partial disabling of a high-speed buffer, or cache, and associated address **index array** and compare circuitry. The arrangement comprises eight rows of 64 entries, each entry in the **index array** being a block **address identifier**, and each entry in the cache being a block of data ( 0 refs.)

**Subfile(s):** C (Computing & Control Engineering)

**Descriptors:** data communication systems; error detection

**Identifiers:** high speed buffer entries; partial deletion; buffer data error; address compare error; disabling process; cache; address **index array**

**Classification Codes:** C5600 (Data communication equipment and techniques)

**INSPEC Update Issue:** 1975-005

**Copyright:** 1975, IEE

**Abstract:** ...shown permits a partial disabling of a high-speed buffer, or cache, and associated address **index array** and compare circuitry. The arrangement comprises eight rows of 64 entries, each entry in the **index array** being a block **address identifier**, and each entry in the cache being a block of data

**Identifiers:** ...speed buffer entries; partial deletion; buffer data error; address compare error; disabling process; cache; address **index array**

#### Dialog eLink:

#### ISPTO Full Text Retrieval Options

11/5,K/7 (Item 1 from file: 34)

DIALOG(R)File 34: SciSearch(R) Cited Ref Sci

(c) 2010 The Thomson Corp. All rights reserved.

05834348 **Genuine Article#:** XA696 **Number of References:** 27

**Title:** Multirate VLSI arrays and their synthesis

**Author:** Lenders P (REPRINT) ; Rajopadhye S

**Corporate Source:** UNIV NEW ENGLAND,DEPT COMP SCI/ARMIDALE/NSW/AUSTRALIA/ (REPRINT); INST RECH INFORMAT & SYST ALEATOIRES,/F-35042 RENNES//FRANCE/

**Journal:** IEEE TRANSACTIONS ON COMPUTERS , 1997 , V 46 , N5 ( MAY ) , P 515-529

**ISSN:** 0018-9340 **Publication Date:** 19970500

**Publisher:** IEEE COMPUTER SOC , 10662 LOS VAQUEROS CIRCLE, PO BOX 3014, LOS ALAMITOS, CA 90720-1314

**Language:** English **Document Type:** ARTICLE

**Geographic Location:** AUSTRALIA; FRANCE

**Subfile:** CC ENGI--Current Contents, Engineering, Computing & Technology

**Journal Subject Category:** ENGINEERING, ELECTRICAL & ELECTRONIC; COMPUTER SCIENCE, HARDWARE & ARCHITECTURE

**Abstract:** Many applications in signal and image processing can be efficiently implemented on regular VLSI architectures such as systolic arrays. Multirate arrays (MRAs) are an extension of systolic arrays where different data streams are propagated with different clocks. We address the **analysis** and synthesis problem for this class of architectures. We present a formal definition of MRAs, as systems of recurrence equations defined over sparse polyhedral domains. We also give transformation rules for this class of recurrences, and use them to show that MRAs constitute a particular subset of systems of affine recurrence equations (SoAREs). We then address the synthesis problem, and show how an MRA can be systematically derived from an initial specification in the form of a mathematical equation. The main transformations that we use are domain rescalings and dependency decomposition, and we illustrate our method by deriving a hitherto unknown decimation filter array.

**Descriptors:** SCIAuthor Keywords: application specific processor **arrays** ; space-time mappings ; **index** transformations ; systolic **arrays** ; VLSI signal processing

**Identifiers:** KeyWord Plus(R): PROCESSOR

#### Cited References:

BALTUS DG, 1993, P428, P INT C APPL SPEC AR

CHEN MC, 1986, PRINCIPLES PROGRAMMI

KARP RM, 1967, V14, P563, J ASSOC COMPUT MACH

KUNG SY, 1982, V31, P1054, IEEE T COMPUT

LENDERS P, 1991, P PAC RIM C COMM COM

LEVERGE H, 1991, V3, P173, J VLSI SIGNAL PROC

LEVERGE H, 1994, RECURRENCES LATTICE

LEVERGE H, 1992, THESIS U RENNES 1 IR  
LI A, 1990, P ICASSP 90 INT C AC  
LI A, 1990, THESIS OREGON STATE  
LI JK, 1991, V13, P213, J PARALLEL DISTR COM  
MARUAS C, 1990, P100, P INT C APPL SPEC AR  
MAURAS C, 1989, THESIS U RENNES 1 IR  
MEAD C, 1980, P271, ALGORITHMS VLSI PROC  
QUINTON P, 1989, V1, P95, J VLSI SIGNAL PROCES  
QUINTON P, 1987, P229, SYSTEMATIC DESIGN SY  
RAJOPADHYE SV, 1990, V14, P163, PARALLEL COMPUT  
RAJOPADHYE SV, 1986, THESIS U UTAH SALT L  
RAO S, 1986, P34, P HIGHL PAR SIGN PRO  
RAO S, 1985, THESIS STANFORD U IN  
ROYCHOWDHURY V, 1988, V3, P459, VLSI SIGNAL PROCESSI  
TEICH J, 1993, V14, P297, INTEGRATION  
WONG FC, 1988, P403, P INT C SYST ARR SAN  
YAACOB Y, 1989, V1, P115, J VLSI SIGNAL PROC  
YAACOB Y, 1988, P AWOC 1988 3 INT WO  
YAACOB Y, 1988, TRC8718 U CAL SANT B  
ZHENG Y, 1993, P692, P ASAP 93 APPL SPEC

**Abstract:** ...an extension of systolic arrays where different data streams are propagated with different clocks. We address the analysis and synthesis problem for this class of architectures. We present a formal definition of MRAs...

**Descriptors:** ...application specific processor arrays ; space-time mappings ; index transformations ; systolic arrays ; VLSI signal processing

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? t/ 5,k/ all

#### Dialog eLink:

#### USPTO Full Text Retrieval Options

9/5,K/1 (Item 1 from file: 56)

DIALOG(R) File 56: Computer and Information Systems Abstracts

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0000934500 IP Accession No: 201001-25-0129545

**When the front line is breached, Ingrian i140 puts up a good fight**

MacVittie, Don

Network Computing , v 13 , n 3 , p 28-29 , 4 Feb. 2002

**Publication Date:** 2002

**Publisher:** CMP Media LLC , 600 Community Drive , Manhasset , NY , 11030

**Country Of Publication:** USA

**Publisher Email:** bevans@cmp.com

**Document Type:** Journal Article

**Record Type:** Abstract

**Language:** English

**ISSN:** 1046-4468

**File Segment:** Computer & Information Systems Abstracts

#### Abstract:

To protect sensitive enduser data traversing your network, the i140 uses RSA to encrypt the data you choose to protect both in your database and on your network. The i140 is placed on your network between the edge router and Web servers. In this strategic location, it encrypts data fields that you specified as sensitive before they are passed to the Web server. The same set of rules lets the i140 decrypt these fields on the way out of your network, making it ideal for public Web site use.

**Descriptors:** Networks; World Wide Web; Servers (computers); Databases; Position (location); Computation; Routers; Websites

**Subj Catg:** 25, Computer Communication Networks  
**Publication Date:** 2002

**Abstract:**

...is placed on your network between the edge router and Web servers. In this strategic **location**, it encrypts data **fields** that you specified as sensitive before they are passed to the **Web server**. The same **set** of rules lets the i140 decrypt these fields on the way out of your network...

**Dialog eLink:**

**ISPTO Full Text Retrieval Options**

9/5,K/2 (Item 2 from file: 56)  
DIALOG(R)File 56: Computer and Information Systems Abstracts  
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0000357247 IP Accession No: 544000

**Supporting object accesses in a Java processor**

Vijaykrishnan, N; Ranganathan, N Pennsylvania State Univ, University Park, PA, USA  
IEE Proceedings: Computers and Digital Techniques , v 147 , n 6 , p 435-443 , Nov. 2000  
**Publication Date:** 2000  
**Publisher:** Institution of Electrical Engineers , Michael Faraday House, Six Hills Way , Stevenage, Herts , SG1 2AY  
**Country Of Publication:** UK  
**Publisher Url:** <http://www.iee.org>  
**Publisher Email:** [esej@iee.org.uk](mailto:esej@iee.org.uk)

**Document Type:** Journal Article

**Record Type:** Abstract

**Language:** English

**ISSN:** 1350-2387

**File Segment:** Computer & Information Systems Abstracts

**Abstract:**

Due to Java's object-based nature and support for garbage collection, efficient object manipulation and relocation are critical to the execution speed of Java code. Java Virtual Machine implementations that utilize handle representation such as Sun's Java Development Kit 1.1 enable efficient object relocation at the cost of an additional indirection for each object access. The direct address object representations such as those used in CACAO and NET compiler eliminate the indirection overhead, but update during object relocation is complex. A virtual address object cache that reduces the indirection overhead while maintaining the efficiency of object relocation is proposed. The objects in the virtual address cache are addressed directly using the object reference and **field offset** pair. This eliminates the indirection overhead and off-set addition overhead associated with the handle representation model. A hardware object table that maintains the handles is used to obtain the actual object location on a virtual address cache miss. The performance of the virtual **address** cache is **analyzed** using various Java programs, and is found to reduce 1.5 cycles per object access on an average as compared to the handle representation model for the various benchmarks studied.

**Descriptors:** Java programming language; Object oriented programming; Buffer storage; Computer hardware

**Identifiers:** Java processor; Object relocation; Java virtual machines

**Subj Catg:** C 723.1, Computer Programming; C 723.1.1, Computer Programming Languages; C 722.1, Data Storage (Equipment and Techniques)

**Publication Date:** 2000

**Abstract:**

...The objects in the virtual address cache are addressed directly using the object reference and **field offset** pair. This eliminates the indirection overhead and off-set addition overhead associated with the handle... ...the actual object location on a virtual address cache miss. The performance of the virtual **address** cache is **analyzed** using various Java programs, and is found to reduce 1.5 cycles per object access ...

9/5,K/3 (Item 1 from file: 35)  
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01797698 ORDER NO: AADAA-19935476

THE IDENTIFICATION OF PRIMARY OPEN ANGLE GLAUCOMA USING MOTION AUTOMATED PERIMETRY (MAP) (RANDOM DOT KINEMATOGAMS)



**Author:** BOSWORTH, CHARLES FLOYD

**Degree:** PH.D.

**Year:** 1999

**Corporate Source/ Institution:** UNIVERSITY OF CALIFORNIA, SAN DIEGO ( 0033 )

**Co-chairs:** DONALD MACLEOD; PAMELA SAMPLE

**Source:** Volume 6006B of Dissertations Abstracts International.

**PAGE** 2621 . 141 PAGES

**Descriptors:** HEALTH SCIENCES, OPHTHALMOLOGY ; PSYCHOLOGY, EXPERIMENTAL

**Descriptor Codes:** 0381; 0623

The studies conducted were designed to evaluate the ability of random-dot motion displays to diagnose glaucoma in a clinical setting and explore theories of selective magnocellular damage in glaucoma. The first four studies address the ability of random-dot motion displays to diagnose glaucoma. The remaining two studies address theories of **selective** magnocellular damage.

The first study examines whether one can differentiate between areas of known visual field loss and areas of known relative field sparing in eyes with primary open angle glaucoma using motion coherence thresholds. Previous experiments using this methodology for the detection of glaucoma reported little diagnostic power. We hypothesized that this lower power was the result of using larger stimulus diameters. The results of the current study indicate that motion coherence thresholds are significantly poorer for areas of vision with existing visual field loss suggesting that a perimetric motion test should be evaluated.

The purpose of the next three studies was to determine if a perimetric motion test utilizing random-dot kinematograms could identify glaucomatous visual field defects in glaucoma patients and patients exhibiting different risk factors for the disease. Motion coherence thresholds at specific locations throughout the whole visual field were significantly elevated in glaucoma patients and patients at elevated risk for the disease. A larger foveal stimulus was unable to distinguish between the different subject groups.

After evaluating the ability of random-dot kinematograms to detect glaucoma, we conducted two studies which compared motion perimetry and short-wavelength automated perimetry in the same patients to test hypotheses of selective magnocellular damage. Both tests successfully identified glaucoma eyes and a percentage of the suspects, and were correlated by **field location** suggesting non-selective glaucomatous damage for different types of ganglion cells.

**Year:** 1999

...address the ability of random-dot motion displays to diagnose glaucoma. The remaining two studies address theories of **selective** magnocellular damage.

The first study examines whether one can differentiate between areas of known visual... ..tests successfully identified glaucoma eyes and a percentage of the suspects, and were correlated by **field location** suggesting non-selective glaucomatous damage for different types of ganglion cells.

9/5,K/4 (Item 2 from file: 35)

DIALOG(R)File 35: Dissertation Abs Online

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01662847 ORDER NO: AAD99-02236

**USING MULTI-STIMULUS VEP SOURCE LOCALIZATION TO OBTAIN A DETAILED RETINOTOPIC MAP OF HUMAN PRIMARY VISUAL CORTEX (VISUAL-EVOKED POTENTIAL)**

**Author:** SLOTNICK, SCOTT DAVID

**Degree:** PH.D.

**Year:** 1998

**Corporate Source/ Institution:** UNIVERSITY OF CALIFORNIA, BERKELEY ( 0028 )

**Chair:** STANLEY A. KLEIN

**Source:** Volume 5908B of Dissertations Abstracts International.

**PAGE** 3939 . 121 PAGES

**Descriptors:** BIOLOGY, NEUROSCIENCE

**Descriptor Codes:** 0317

Using positron emission tomography and functional magnetic resonant imaging, spatially detailed retinotopic maps of early visual areas in humans have been produced; however, these methods are limited in their temporal resolution. To obtain the temporal response characteristics of neural activation, techniques such as magnetoencephalography and visual-evoked potential (VEP) recording must be used. Unfortunately, acquiring sufficient signal-to-noise using these methods requires a high number of repeated stimuli at each probed **location** across the visual **field** thereby limiting the number of **field positions** that can be mapped onto cortex.

To **address** this limitation, a multi-stimulus array spanning the central 18 degrees of the visual field was used where each of 60 checkerboard stimulus "patches" was simultaneously modulated with an orthogonal m-sequence. VEPs were recorded from a dense posterior electrode array. The response across the electrode array due to each patch was computed by cross-correlating the m-sequence of the patch of interest with the response of each electrode (Sutter, 1992). For each stimulus patch, single dipole source localization was conducted to determine the location, magnitude, and time-function of the underlying neural activation. The locus of the dipole solutions followed a retinotopic pattern which matched the known organization of primary visual cortex

reasonably well. These results provide much better temporal resolution for retinotopic brain sources than previous neuroimaging methods. In addition, this technique has been used to study the neuromodulatory effect of shifts in spatial attention.

**Year: 1998**

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To **address** this **limitation**, a multi-stimulus array spanning the central 18 degrees of the visual field was used...

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9/5,K/5 (Item 1 from file: 2)

DIALOG(R)File 2: INSPEC

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06213235

**Title:** Determination of starting shock velocity in supersonic wind tunnel

**Author(s):** Disimile, P.J.; Toy, N.

**Author Affiliation:** Cincinnati Univ., OH, USA

**Journal:** AIAA Journal , vol.33 , no.10 , pp.1981-3

**Publisher:** AIAA

**Country of Publication:** USA

**Publication Date:** Oct. 1995

**ISSN:** 0001-1452

**SI CI:** 0001-1452(199510)33:10L:1981:DSSV;1-F

**CODEN:** AIAJAH

**U.S. Copyright Clearance Center Code:** 0001-1452/95/\$2.00+.50

**Language:** English

**Document Type:** Journal Paper (JP)

**Treatment:** Experimental (X)

**Abstract:** In the case of many high-speed facilities, the nominal experimental run time is often on the order of seconds or minutes before the facility air is exhausted. During this time the tunnel parameters have to stabilize before measurements are taken, and it is this time period that is very important to the tunnel operating conditions. For supersonic/hypersonic tunnels this time period is related to the passing of the starting shock through the working section, and in many applications this has to be inferred from pressure measurements. Although these techniques are well established, they are generally only point measurements. In the case of an inclined shock, probe or tap location would bias the measurement; therefore, a full-field technique would be advantageous. It is this particular area that the technique of using liquid crystals is to **address**, in particular to **evaluate** the speed of the shock wave as the tunnel is started. The method relies upon coating the surface of the tunnel wall with a thin layer of liquid crystal and illuminating the surface with white light while viewing with a color charge-coupled device (CCD) camera ( 6 refs.)

**Subfile(s):** A (Physics)

**Descriptors:** flow measurement; shock waves; supersonic flow; velocity measurement; wind tunnels

**Identifiers:** parameter stabilisation; probe location; shock wave speed; colour charge-coupled device camera; CCD camera; starting shock velocity; supersonic wind tunnel; run time; facility air; tunnel parameters; time period; working section; pressure measurements; tap **location**; full- **field** technique; liquid crystals; white light

**Classification Codes:** A4780 (Measurement instrumentation and techniques for fluid dynamics); A4740K (Supersonic and hypersonic flows); A4740N (Shock-wave interactions); A4760 (Flows in ducts, channels, and conduits)

**INSPEC Update Issue:** 1996-011

**Copyright:** 1996, IEE

**Abstract:** ...advantageous. It is this particular area that the technique of using liquid crystals is to **address**, in particular to **evaluate** the speed of the shock wave as the tunnel is started. The method relies upon...

**Identifiers:** ...wind tunnel; run time; facility air; tunnel parameters; time period ; working section; pressure measurements; tap **location**; full- **field** technique; liquid crystals; white light (19951000)

**Dialog eLink:**

**USPTO Full Text Retrieval Options**

9/5,K/6 (Item 2 from file: 2)

DIALOG(R)File 2: INSPEC

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05264665

**Title:** Built-in self-diagnostic read-only-memories

**Author(s):** Nagvajara, P.; Karpovsky, M.G.  
**Author Affiliation:** Dept. of Electr. & Comput. Eng., Drexel Univ., Philadelphia, PA, USA  
**Inclusive Page Numbers:** 695-703  
**Publisher:** Int. Test Conference, Altoona, PA  
**Country of Publication:** USA  
**Publication Date:** 1991  
**Conference Title:** Proceedings. International Test Conference 1991 (IEEE Cat. No.91CH3032-0)  
**Conference Date:** 26-30 Oct. 1991  
**Conference Location:** Nashville, TN, USA  
**Conference Sponsor:** IEEE  
**ISBN:** 0 8186 9156 5  
**U.S. Copyright Clearance Center Code:** CH3032-0/91/0000-0695\$01.00  
**Number of Pages:** xiv+1135  
**Language:** English  
**Document Type:** Conference Paper (PA)  
**Treatment:** Practical (P)

**Abstract:** A design of built-in self-diagnostic read only memories (ROMs) which extends the concept of the built-in self-test to provide fault-masking in the ROM normal operating mode is presented. Switch-level fault analysis of the ROMs showed that most of the single transistor stuck-open/on faults (on the order of 95% or more) will result in errors confined in the content of a single **address**. The diagnostic scheme **identifies** these errors and locates the address for which the data are corrupted. In the ROM operating mode errors are corrected at the ROM outputs when the content of corresponding address is read. A VLSI implementation is presented where the area overhead is estimated to be on the order of 15% or less ( 22 refs.)

**Subfile(s):** B (Electrical & Electronic Engineering); C (Computing & Control Engineering); E (Mechanical & Production Engineering)

**Descriptors:** built-in self test; CMOS integrated circuits; fault **location**; insulated gate **field** effect transistors; integrated circuit testing; integrated memory circuits; logic testing; read-only storage; VLSI

**Identifiers:** switch level fault analysis; BIST; built-in self-diagnostic read only memories; built-in self-test; fault-masking; ROM; fault analysis; stuck-open/on faults; VLSI

**Classification Codes:** B1265D (Memory circuits); B0170E (Production facilities and engineering); B7210B (Computerised instrumentation); B1265B (Logic circuits); B2570D (CMOS integrated circuits); C5320G (Semiconductor storage); C5210 (Logic design methods); E1520 (Manufacturing processes); E1630 (Testing); E1640 (Instrumentation)

**INSPEC Update Issue:** 1992-047

**Copyright:** 1992, IEE

**Abstract:** ...of 95% or more) will result in errors confined in the content of a single **address**. The diagnostic scheme **identifies** these errors and locates the address for which the data are corrupted. In the ROM...

**Descriptors:** built-in self test; CMOS integrated circuits; fault **location**; insulated gate **field** effect transistors; integrated circuit testing; integrated memory circuits; logic testing; read-only storage; VLSI (19910000)

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9/5,K/7 (Item 3 from file: 2)

DIALOG(R) File 2: INSPEC

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02109015

**Title:** Pattern generator for a multipart number test system

**Author(s):** Arnold, J.N.; Czepiel, R.J.; Prilik, R.J.; Smith, E.A.

**Author Affiliation:** IBM Corp., Armonk, NY, USA

**Journal:** IBM Technical Disclosure Bulletin, vol.19, no.9, pp.3487-8

**Country of Publication:** USA

**Publication Date:** Feb. 1977

**ISSN:** 0018-8689

**CODEN:** IBMTAA

**Language:** English

**Document Type:** Journal Paper (JP)

**Treatment:** Practical (P)

**Abstract:** An address counter is employed in an array test exerciser to generate the bit address for the memory cells tested, the read/write command, the data-in pattern, chip select or module select and the data output line selection by imposing a binary incrementation or decrementation in a conventional counter whose sequence of binary bit **positions** is designated as **fields** which control the respective functions of address generation read/write, pattern control, chip select or output line enable ( 0 refs.)

**Subfile(s):** C (Computing & Control Engineering)

**Descriptors:** cellular arrays; computer testing; counting circuits

**Identifiers:** multipart number **test** system; **address** counter; array **test** exerciser; memory cells; read/write command; chip select; module select; data output line selection; pattern control

**Classification Codes:** C6150G (Diagnostic, testing, debugging and evaluating systems)

**INSPEC Update Issue:** 1977-009

**Copyright:** 1977, IEE

**Abstract:** ...imposing a binary incrementation or decrementation in a conventional counter whose sequence of binary bit **positions** is designated as **fields** which control the respective functions of address generation read/write, pattern control, chip select or...

**Identifiers:** multipart number **test** system; **address** counter; array **test** exerciser; memory cells; read/write command; chip select; module select; data output line selection; pattern... (19770200)

**Dialog eLink:** [Check for PDF Download Availability and Purchase](#)

9/5,K/8 (Item 1 from file: 6)

DIALOG(R) File 6: NTIS

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1416598 **NTIS Accession Number:** DE88703768

**Modular System for Spectroscopic Data Acquisition. Multi-Channel Analyzer**

Boja, Y. ; Vagov, V. A. ; Zhukov, G. P. ; Rubin, D. ; Kharangozo, Z.

Joint Inst. for Nuclear Research, Dubna (USSR). Lab. of Neutron Physics.

**Corporate Source Codes:** 014897003; 3473000

**Report Number:** JINR-R-10-87-691

1987 19p

**Language:** Russian

**Journal Announcement:** GRAI8908

In Russian.

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**NTIS Prices:** PC A03/MF A01

**Country of Publication:** Union of Soviet Socialist Republics

A Multichannel Analyzer of the CAMAC data acquisition system having modular architecture is described. It is intended for experimental data processing: receiving analyzing and storing. The system provides setting of: 4K volume memory address **field**; **offset** of memory working **field**; **address** and data overflow **test**; word length of memory 12/24 bit; data block and word transmission in programmable way. The maximum memory capacity of the analyzer is 32Kx24 bit and the memory cycle time is at least 2  $\mu$ s. 3 refs.; 5 figs. (Atomindex citation 19:073275)

**Descriptors:** \* Multi-Channel Analyzers; \* CAMAC System; \* Data Acquisition Systems; Data Processing; Data Transmission; Equipment Interfaces; Flowsheets; Spectrometers

**Identifiers:** \* Foreign technology; ERDA/440103; Pulse height analyzers; NTISINIS

**Section Headings:** 88B (Library and Information Sciences--Information Systems); 62B (Computers, Control, and Information Theory--Computer Software)

...data processing: receiving analyzing and storing. The system provides setting of: 4K volume memory address **field**; **offset** of memory working **field**; **address** and data overflow **test**; word length of memory 12/24 bit; data block and word transmission in programmable way...

**Descriptors:**

